NCR

NCR45CG72

GEOMETRIC ARITHMETIC PARALLEL PROCESSOR

■ APPLICATIONS

- PATTERN RECOGNITION
  - Correlation
  - Sobel Transform
  - Spoke Filter
  - Template Matching
  - Automated Inspection
  - Machine Vision
- PARALLEL DATA PROCESSING
  - Convolution
  - Matrix Operations
  - Histogram
  - Search and Sort
- IMAGE PROCESSING
  - Image Enhancement
  - Edge Detection
  - 2-Dimensional Convolution
  - Compression
  - Spatial Filtering
  - Differential Imaging
- ASSOCIATIVE PROCESSOR
  - Content Addressable Memory
  - Limit Search
  - Hamming Distance

■ GENERAL DESCRIPTION

The NCR45CG72 is a two-dimensional systolic array processor chip. It is a mesh-connected six by twelve arrangement of 1 bit processor elements. Each processor element can communicate with four neighbors: N,E,S, and W. Each processor element is composed of a bit serial ALU, 128 X 1 bit RAM and 4 single bit latches: Three latches hold inputs to the ALU and the fourth latch allows I/O through the cell without interrupting the ALU, i.e. I/O operations are overlapped with computation.

The cascadeability of the GAPP allows system designers to implement arrays of processors of arbitrary size in multiples of 6 X 12 elements.

■ FEATURES

- CMOS systolic array with 72 processors per chip
- 6 X 12 array of bit serial processor elements
- Single instruction multiple data stream architecture — all processor elements operate in parallel
- GAPP devices are fully cascadeable
- System throughput increases linearly with number of processor elements in the system
- Broadcast giobal input and output
- Separate I/O bus = overlapped I/O and computation
- 128 Bits of static RAM per processor
- VLSI double layer metal CMOS technology
- 500 milliwatts power at 10 MHz

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■ ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} . . . . . + 7V

Voltage on any pin with respect to ground. . . . . −0.3 to V_{DD} + 0.3V

Storage temperature. . . . . −65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operation conditions stipulated elsewhere in this specification is not implied.

CAUTION

1. CMOS Devices are damaged by high energy electrostatic discharge. Devices must be stored in conductive foam or with all pins shunted. Precautions should be taken to avoid application of voltages higher than the maximum rating.
2. Remove power before insertion or removal of this device.

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Supply Current (10 pF loads)					
45CG72-2		–		80	mA
45CG72-1	I_{DD}	–		100	mA
Input Low Voltage	V_{IL}	0.0		0.8	V
Input High Voltage	V_{IH}	2.0		V_{DD}	V
Output Low Voltage (I_{OL} = 2 mA)	V_{OL}	–		0.4	V
Output High Voltage (I_{OH} = 1 mA)	V_{OH}	2.4		–	V
Temperature	T_A	0		70	°C
Input Capacitance	C_{IN}	–		8	pF
Output Capacitance	C_O	–		8	pF
Leakage Current on any Input or I/O Pin	I_{IN}	–		10	μA

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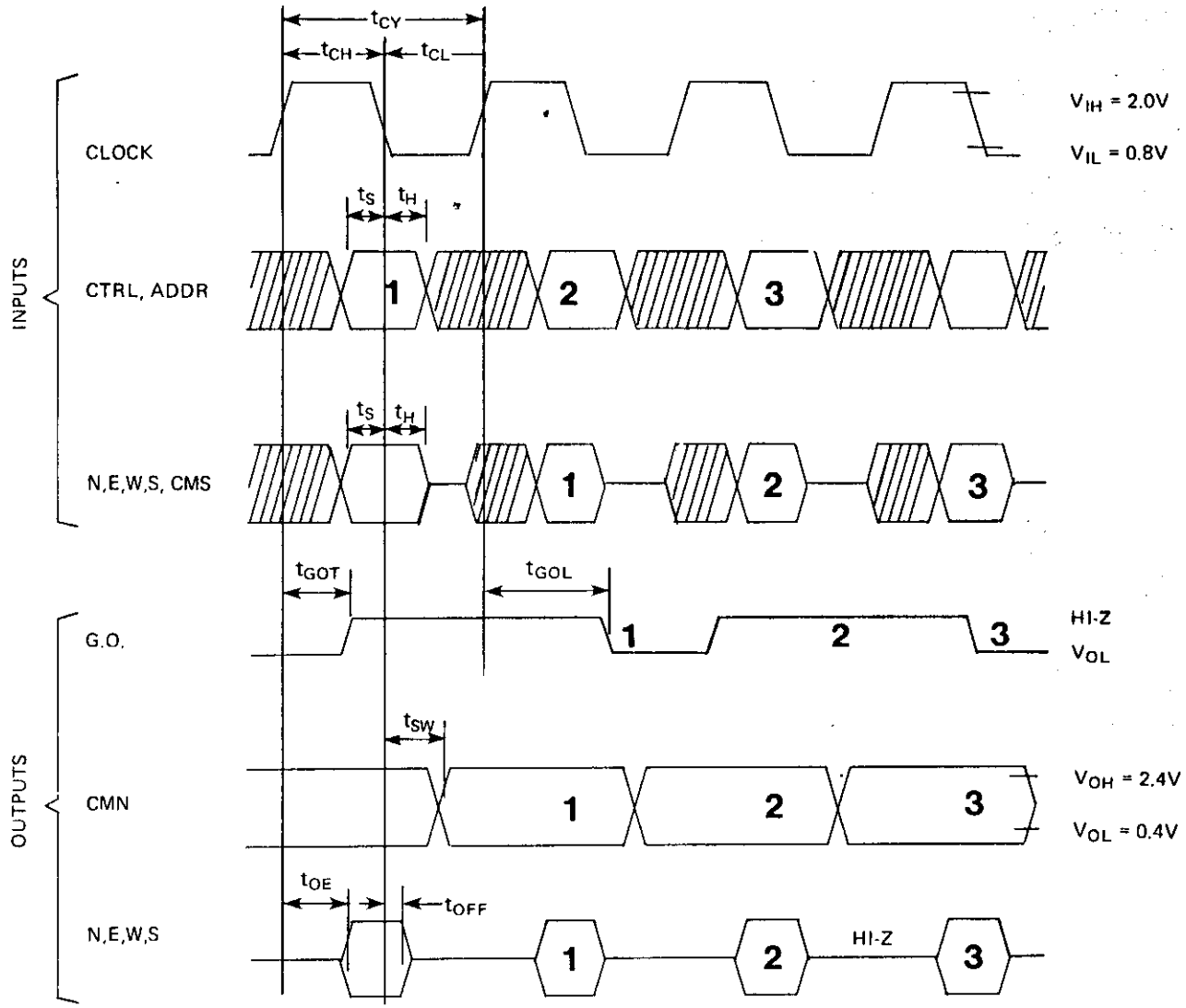
■ TIMING DIAGRAM



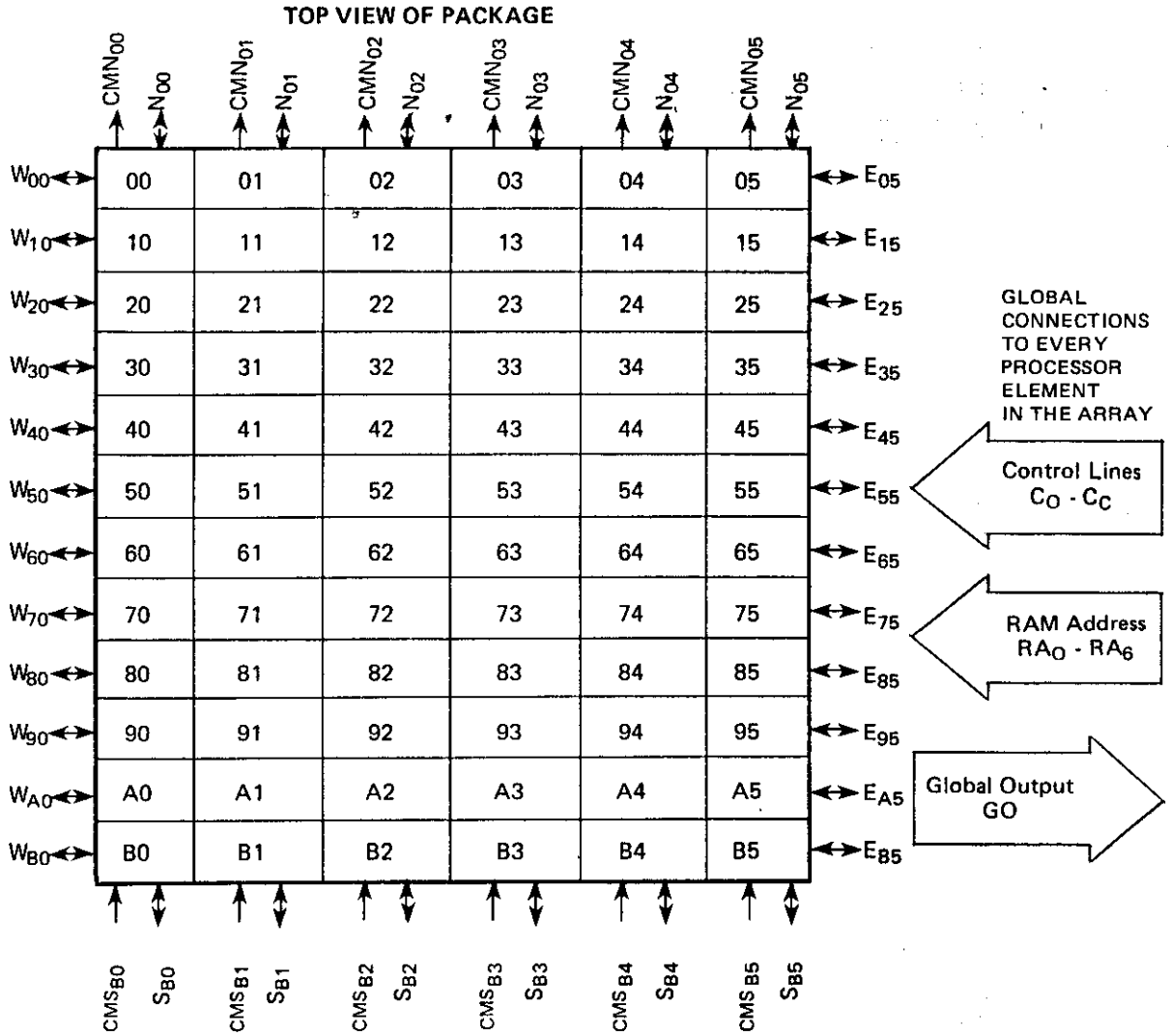
NOTE: 1,2,3 refer to the staging sequence of instruction, data in and data out.

■ AC CHARACTERISTICS

PARAMETER	SYMBOL	NCR45CG72-2		NCR45CG72-1		
		MIN	MAX	MIN	MAX	UNITS
CYCLE TIME	t_{CY}	200		100		ns
CLOCK LOW	t_{CL}	100	5000	50	5000	ns
CLOCK HIGH	t_{CH}	100	5000(1)	50	5000(1)	ns
SETUP TIME	t_S	20		10		ns
INPUT HOLD TIME	t_H	10		10		ns
OUTPUTS ENABLED	t_{OE}	10	50	10	35	ns
OUTPUT HOLD TIME	t_{OFF}	10	50	10	30	ns
GLOBAL OUTPUT LOW	t_{GOL}	20	100	10	70	ns
GLOBAL OUTPUT TRISTATE	t_{GOT}	10	50	10	35	ns
CMN OUTPUT	t_{SW}	20	120	10	85	ns

NOTE: (1) d.c. by design; tested at 5 μsec.

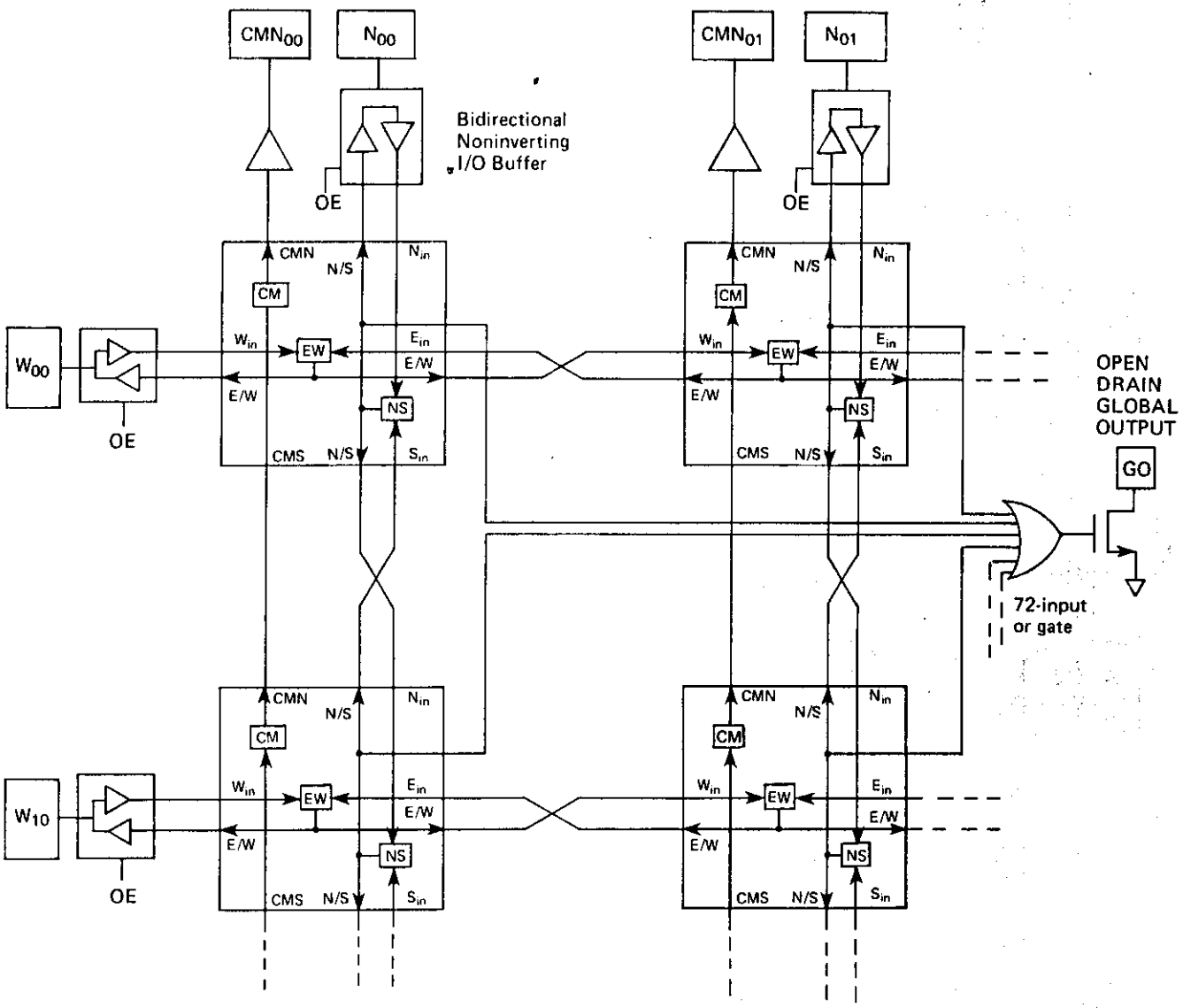
■ PROCESSOR ELEMENT AND DATA BUS IDENTIFICATION



NOTE: This numbering scheme may be extended in systems which contain more than one GAPP device.

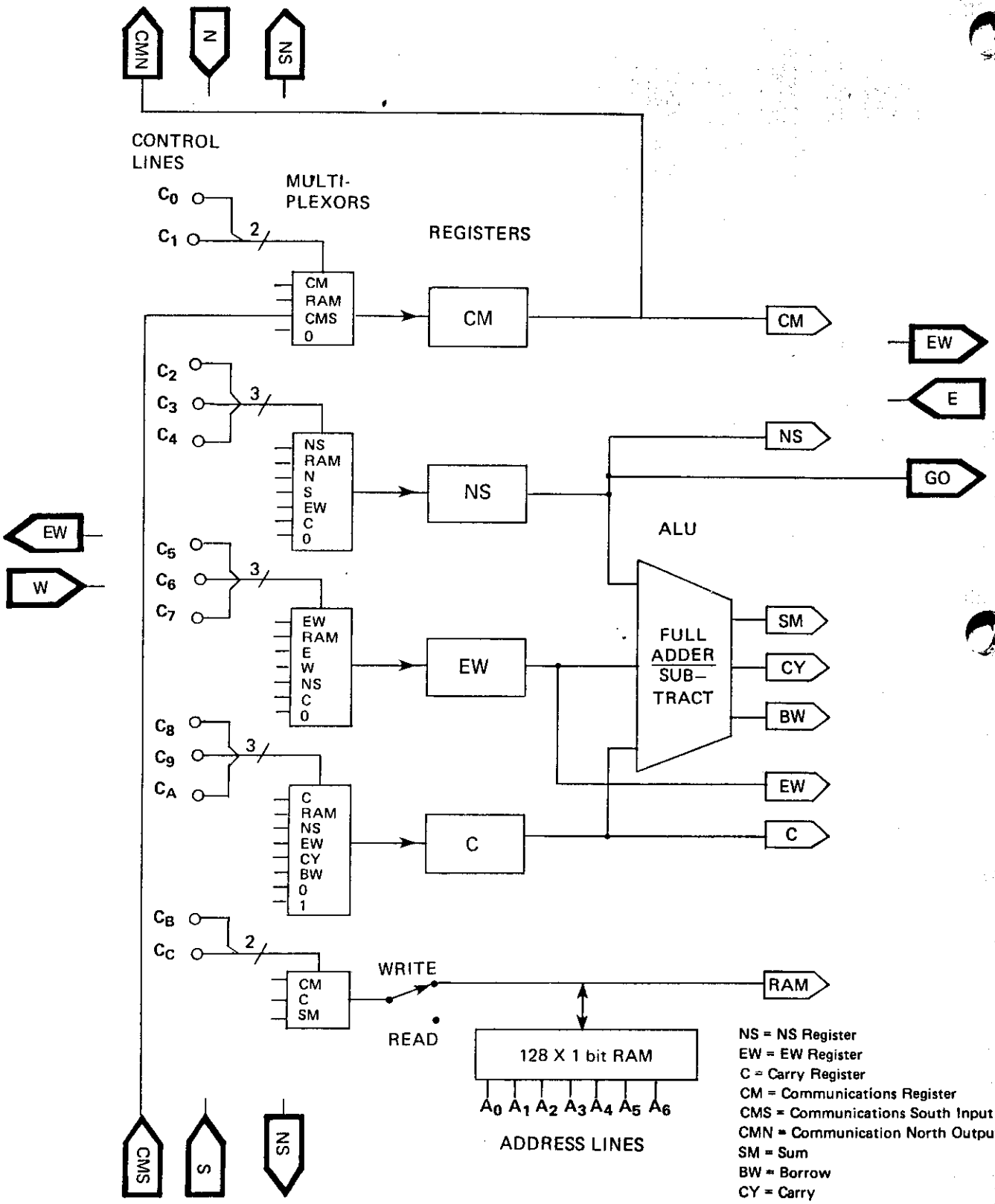
PIN LABELS	
$W_{00} - W_{B0}$	WEST DATA BUS
$E_{05} - E_{B5}$	EAST DATA BUS
$N_{00} - N_{05}$	NORTH DATA BUS
$S_{B0} - S_{B5}$	SOUTH DATA BUS
$CMS_{B0} - CMS_{B5}$	INPUT BUS
$CMN_{00} - CMN_{05}$	OUTPUT BUS
$RA_0 - RA_6$	RAM ADDRESS BUS
$C_0 - C_C$	CONTROL LINES – INSTRUCTION BUS – GLOBAL DATA INPUT BUS
GO	GLOBAL OUTPUT LINE

■ BLOCK DIAGRAM OF CONNECTIONS BETWEEN FOUR PROCESSOR ELEMENTS



OE = Output Enable is an internal connection.
East Outputs enabled whenever EW:=W
West Outputs enabled whenever EW:=E
North Outputs enabled whenever NS:=S
South Outputs enabled whenever NS:=N
GO is pulled low whenever any NS register contains 1

■ SCHEMATIC DIAGRAM OF ONE PROCESSOR ELEMENT



■ INSTRUCTION SET

Register Operation	Mnemonic	Control Lines C_C	C_B	C_A	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	Description
CM	CM: = CM	X	X	X	X	X	X	X	X	X	X	X	0	0	MICRO-NOP
	CM: = RAM	X	X	X	X	X	X	X	X	X	X	X	0	1	LOAD CM FROM RAM
	CM: = CMS	X	X	X	X	X	X	X	X	X	X	X	1	0	MOVE FROM CMS INTO CM
	CM: = 0	X	X	X	X	X	X	X	X	X	X	X	1	1	LOAD Ø INTO CM
NS	NS: = NS	X	X	X	X	X	X	X	X	0	0	0	X	X	MICRO-NOP
	NS: = RAM	X	X	X	X	X	X	X	X	0	0	1	X	X	LOAD NS FROM RAM
	NS: = N	X	X	X	X	X	X	X	X	0	1	0	X	X	MOVE FROM N INTO NS
	NS: = S	X	X	X	X	X	X	X	X	0	1	1	X	X	MOVE FROM S INTO NS
	NS: = EW	X	X	X	X	X	X	X	X	1	0	0	X	X	MOVE FROM EW INTO NS
	NS: = C	X	X	X	X	X	X	X	X	1	0	1	X	X	MOVE FROM C INTO NS
	NS: = 0	X	X	X	X	X	X	X	X	1	1	0	X	X	LOAD Ø INTO NS
EW	EW: = EW	X	X	X	X	X	0	0	0	X	X	X	X	X	MICRO-NOP
	EW: = RAM	X	X	X	X	X	0	0	1	X	X	X	X	X	LOAD EW FROM RAM
	EW: = E	X	X	X	X	X	0	1	0	X	X	X	X	X	MOVE FROM E INTO EW
	EW: = W	X	X	X	X	X	0	1	1	X	X	X	X	X	MOVE FROM W INTO EW
	EW: = NS	X	X	X	X	X	1	0	0	X	X	X	X	X	MOVE FROM NS INTO EW
	EW: = C	X	X	X	X	X	1	0	1	X	X	X	X	X	MOVE FROM C INTO EW
	EW: = 0	X	X	X	X	X	1	1	0	X	X	X	X	X	LOAD Ø INTO EW
C	C: = C	X	X	0	0	0	X	X	X	X	X	X	X	X	MICRO-NOP
	C: = RAM	X	X	0	0	1	X	X	X	X	X	X	X	X	LOAD C FROM RAM
	C: = NS	X	X	0	1	0	X	X	X	X	X	X	X	X	MOVE FROM NS INTO C
	C: = EW	X	X	0	1	1	X	X	X	X	X	X	X	X	MOVE FROM EW INTO C
	C: = CY	X	X	1	0	0	X	X	X	X	X	X	X	X	LOAD C FROM CARRY
	C: = BW	X	X	1	0	1	X	X	X	X	X	X	X	X	LOAD C FROM BORROW
	C: = 0	X	X	1	1	0	X	X	X	X	X	X	X	X	LOAD Ø INTO C
	C: = 1	X	X	1	1	1	X	X	X	X	X	X	X	X	LOAD 1 INTO C
RAM	READ	0	0	X	X	X	X	X	X	X	X	X	X	X	READ FROM RAM
	RAM: = CM	0	1	X	X	X	X	X	X	X	X	X	X	X	LOAD RAM FROM CM
	RAM: = C	1	0	X	X	X	X	X	X	X	X	X	X	X	LOAD RAM FROM C
	RAM: = SM	1	1	X	X	X	X	X	X	X	X	X	X	X	LOAD RAM FROM SUM

■ ARITHMETIC OPERATIONS

Adder/Subtracter Operations

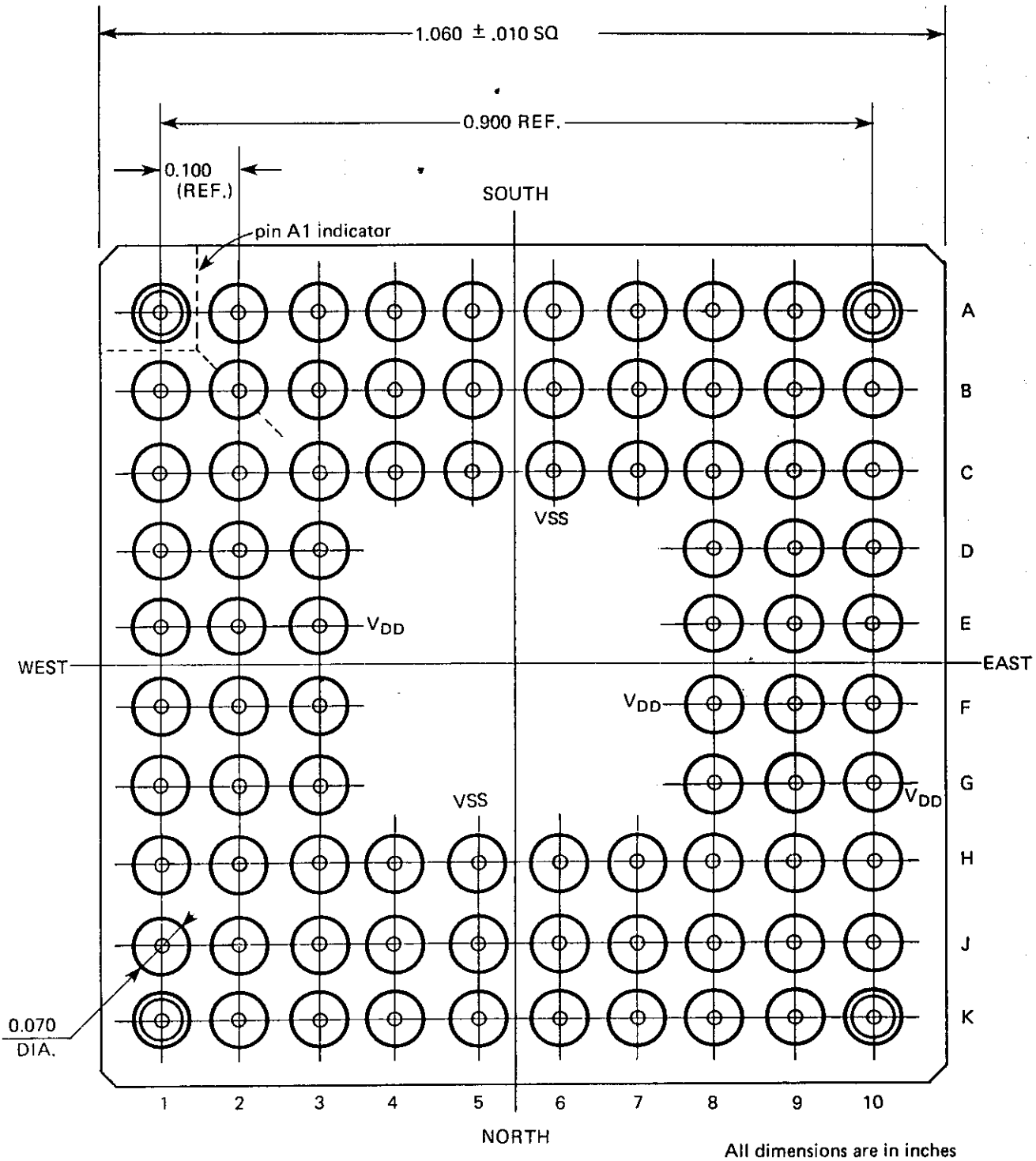
INPUT			OUTPUT		
NS	EW	C	SM	CY	BW
0	0	0	0	0	0
0	1	0	1	0	1
1	0	0	1	0	0
1	1	0	0	1	0
0	0	1	1	0	1
0	1	1	0	1	1
1	0	1	0	1	0
1	1	1	1	1	1

■ LOGIC OPERATIONS

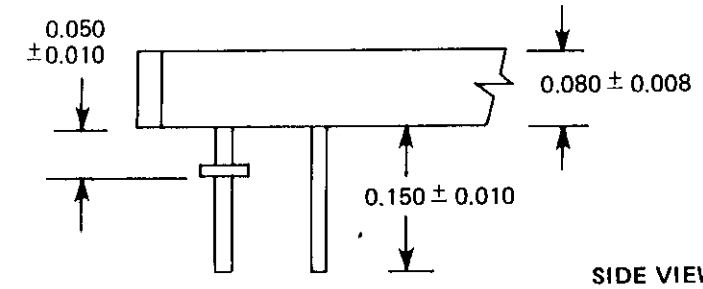
LOGICAL OPERATION	DESCRIPTION	CONDITIONS
INV	$SM = \overline{NS}$	EW = 0, C = 1
	$SM = \overline{EW}$	NS = 0, C = 1
	$SM = \overline{C}$	NS = 0, EW = 1
AND	$CY = NS \bullet EW$	C = 0
	$CY = EW \bullet C$	NS = 0
	$CY = NS \bullet C$	EW = 0
	$BW = \overline{NS} \bullet EW$	C = 0
OR	$CY = NS + EW$	C = 1
	$BW = \overline{NS} + EW$	C = 1
	$BW = EW + C$	NS = 0
XOR	$SM = NS \oplus C$	EW = 0
	$SM = NS \oplus EW$	C = 0
	$SM = EW \oplus C$	NS = 0
XNOR	$SM = \overline{NS \oplus EW}$	C = 1

■ CERAMIC PIN GRID ARRAY PACKAGE

BOTTOM VIEW



All dimensions are in inches



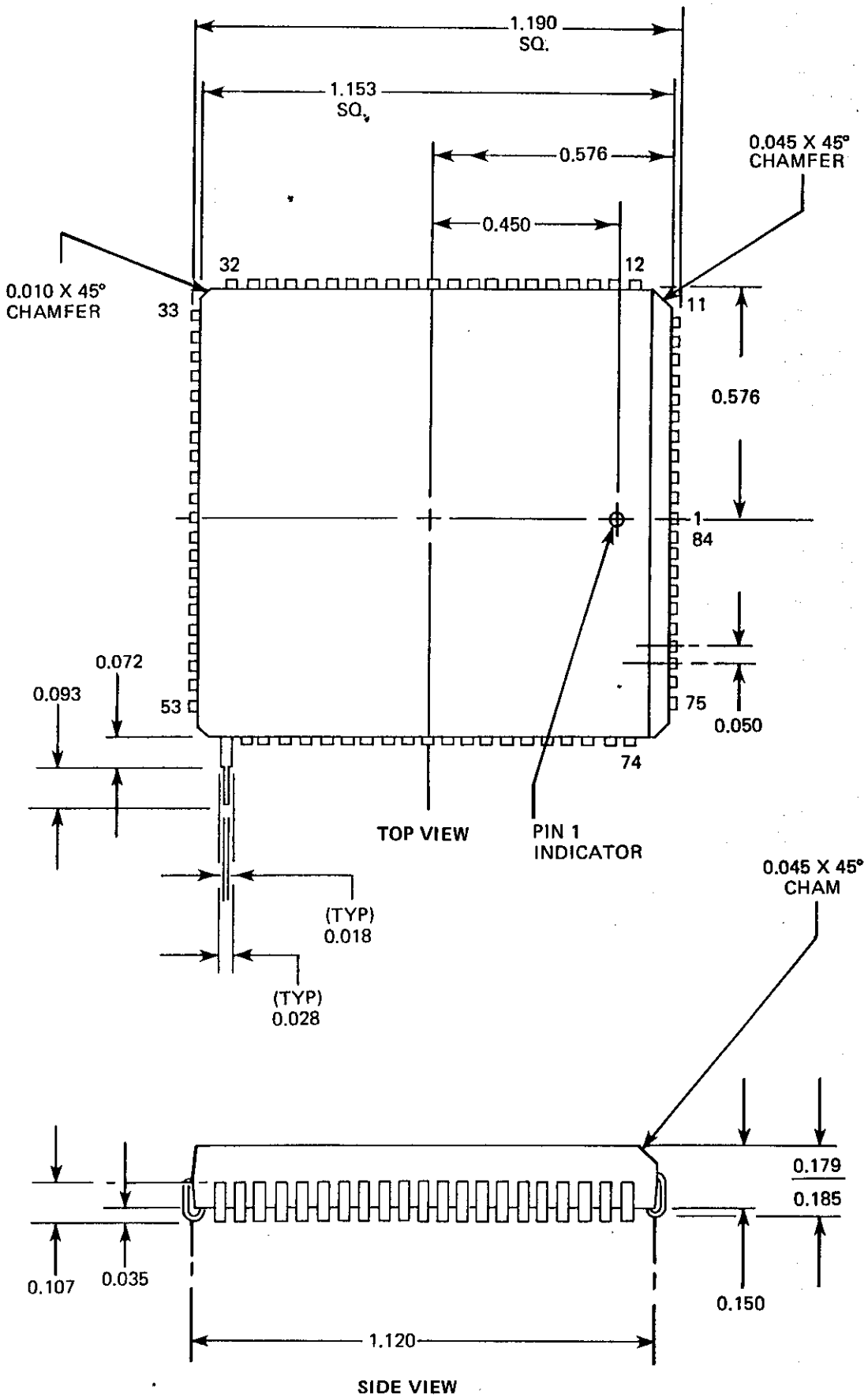
SIDE VIEW

■ TABLE OF PIN NUMBERS VS. SIGNAL LABELS (PLASTIC CHIP CARRIER)

PIN NO.	LABEL	PIN NO.	LABEL	PIN NO.	LABEL
1	NC	29	CMS_{B5}	57	CMN_{05}
2	NC	30	C_8	58	N_{05}
3	NC	31	C_9	59	CMN_{04}
4	W_{60}	32	C_A	60	N_{04}
5	W_{70}	33	C_B	61	CMN_{03}
6	W_{80}	34	C_C	62	N_{03}
7	W_{90}	35	E_{B5}	63	CLK
8	W_{A0}	36	E_{A5}	64	VSS
9	W_{B0}	37	E_{95}	65	RA_5
10	C_2	38	E_{85}	66	RA_3
11	C_3	39	E_{75}	67	RA_1
12	C_4	40	E_{65}	68	CMN_{02}
13	S_{B0}	41	VDD	69	N_{02}
14	CMS_{B0}	42	NC	70	CMN_{01}
15	S_{B1}	43	NC	71	N_{01}
16	CMS_{B1}	44	NC	72	CMN_{00}
17	S_{B2}	45	VDD	73	N_{00}
18	CMS_{B2}	46	E_{55}	74	C_1
19	RA_0	47	E_{45}	75	C_0
20	RA_2	48	E_{35}	76	W_{00}
21	RA_4	49	E_{25}	77	W_{10}
22	VSS	50	E_{15}	78	W_{20}
23	RA_6	51	E_{05}	79	W_{30}
24	S_{B3}	52	C_7	80	W_{40}
25	CMS_{B3}	53	$VDD_{(sub)}$	81	W_{50}
26	S_{B4}	54	GO	82	VDD
27	CMS_{B4}	55	C_6	83	NC
28	S_{B5}	56	C_5	84	NC

NC = No Connection

▪ PLASTIC CHIP CARRIER PACKAGE

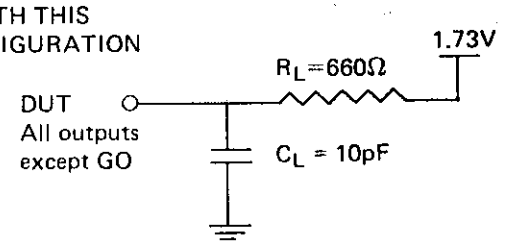


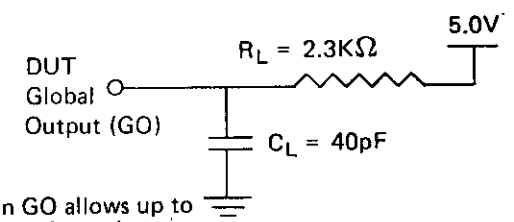
All dimensions are in inches

■ TABLE OF SIGNAL NAMES VS. PIN NUMBERS (CERAMIC AND PLASTIC)

SIGNAL NAMES	CER PIN	PLA PIN	SIGNAL NAMES	CER PIN	PLA PIN	SIGNAL NAMES	CER PIN	PLA PIN
CMS_{B0}	B3	14	N_{04}	K7	60	C_7	J9	52
CMS_{B1}	C4	16	N_{05}	H7	58	C_8	A10	30
CMS_{B2}	A4	18	S_{B0}	A2	13	C_9	C7	31
CMS_{B3}	A9	25	S_{B1}	A3	15	C_A	B9	32
CMS_{B4}	A6	27	S_{B2}	B4	17	C_B	C8	33
CNS_{B5}	B8	29	S_{B3}	A8	24	C_C	B10	34
CMN_{00}	K1	72	S_{B4}	B6	26	RA_0	C5	19
CMN_{01}	J4	70	S_{B5}	B7	28	RA_1	K2	67
CMN_{02}	J5	68	W_{00}	J1	76	RA_2	B5	20
CMN_{03}	H6	61	W_{10}	H2	77	RA_3	K3	66
CMN_{04}	J7	59	W_{20}	H1	78	RA_4	A5	21
CMN_{05}	K8	57	W_{30}	G3	79	RA_5	K4	65
E_{05}	G8	51	W_{40}	G1	80	RA_6	A7	23
E_{15}	K10	50	W_{50}	F3	81	GO	J8	54
E_{25}	H9	49	W_{60}	D1	4	VSS	C6	22
E_{35}	G9	48	W_{70}	C1	5	VSS	H5	64
E_{45}	F9	47	W_{80}	E2	6	VDD	E3	82
E_{55}	J10	46	W_{90}	E1	7	VDD	F8	41
E_{65}	E10	40	W_{A0}	C2	8	VDD	G10	45
E_{75}	E9	39	W_{B0}	A1	9	$VDD_{(sub)}$	–	53
E_{85}	D10	38	CLK	K6	63	N.C.	B1	1
E_{95}	D9	37	C_0	H3	75	N.C.	D2	2
E_{A5}	C10	36	C_1	J2	74	N.C.	D8	3
E_{B5}	C9	35	C_2	D3	10	N.C.	E8	42
N_{00}	H4	73	C_3	B2	11	N.C.	F1	43
N_{01}	J3	71	C_4	C3	12	N.C.	F2	44
N_{02}	K5	69	C_5	K9	56	N.C.	F10	83
N_{03}	J6	62	C_6	H8	55	N.C.	G2	84
						N.C.	H10	–

DEVICES TESTED WITH THIS OUTPUT LOAD CONFIGURATION





Open drain output on GO allows up to 4 devices to be connected together.

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